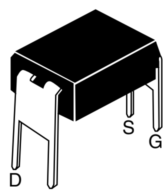
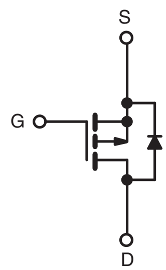
Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	- 50	
$R_{DS(on)}$ (Ω)	V_{GS} = - 10 V	0.50
Q_g (Max.) (nC)	11	
Q_{gs} (nC)	3.8	
Q_{gd} (nC)	4.1	
Configuration	Single	

HVMDIP





P-Channel MOSFET

FEATURES

- For Automatic Insertion
- Compact, End Stackable
- Fast Switching
- Low Drive Current
- Easy Paralleled
- Excellent Temperature Stability
- P-Channel Versatility
- Compliant to RoHS Directive 2002/95/EC

Pb Available
RoHS*
COMPLIANT

DESCRIPTION

The HVMDIP technology is the key to Vishay's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HVMDIP design achieves very low on-state resistance combined with high transconductance and extreme device ruggedness.

The p-channel HVMDIPs are designed for application which require the convenience of reverse polarity operation. They retain all of the features of the more common n-channel HVMDIPs such as voltage control, very fast switching, ease of paralleling, and excellent temperature stability.

P-channels HVMDIPs are intended for use in power stages where complementary symmetry with n-channel devices offers circuit simplification. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuits and pulse amplifiers.

ORDERING INFORMATION	
Package	HVMDIP
Lead (Pb)-free	IRFD9010PbF
	SiHFD9010-E3
SnPb	IRFD9010
	SiHFD9010

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

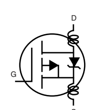
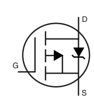
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	- 50	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at - 10 V	T_C = 25 °C	I_D	- 1.1	A
		T_C = 100 °C		- 0.68	
Pulsed Drain Current[a]			I_{DM}	- 8.8	
Linear Derating Factor				0.01	W/°C
Inductive Current, Clamped	L = 100 µH see fig. 14		I_{LM}	- 8.8	A
Inductive Current, Unclamped (Avalanche Current)	see fig. 15		I_L	- 1.5	
Maximum Power Dissipation	T_C = 25 °C		P_D	1	W
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300[d]	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. V_{DD} = - 25 V, starting T_J = 25 °C, L = 52 mH, R_g = 25 Ω, I_{AS} = - 2.0 A (see fig. 12).
c. $I_{SD} \leq$ - 4.0 A, dI/dt ≤ 75 A/µs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 175 °C.
d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	120	°C/W

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 μA		- 50	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = - 1 mA		-	- 0.091	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = - 250 μA		- 2.0	-	- 4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V		-	-	± 500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 50 V, V_{GS} = 0 V		-	-	- 250	μA
		V_{DS} = - 40 V, V_{GS} = 0 V, T_J = 125 °C		-	-	- 1000	
On-State Drain Current	$I_{D(on)}$	V_{GS} = 10 V	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max.	- 1.1	-	-	A
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = - 10 V	I_D = - 0.58 A[b]	-	0.35	0.50	Ω
Forward Transconductance	g_{fs}	V_{DS} = - 20 V, I_D = - 2.4 A		1.7	2.5	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = - 25 V, f = 1.0 MHz, see fig. 5		-	240	-	pF
Output Capacitance	C_{oss}			-	160	-	
Reverse Transfer Capacitance	C_{rss}			-	30	-	
Total Gate Charge	Q_g	V_{GS} = - 10 V	I_D = - 4.7 A, V_{DS} = 0.8 V see fig. 6 and 13[b]	-	7.2	11	nC
Gate-Source Charge	Q_{gs}			-	2.5	3.8	
Gate-Drain Charge	Q_{gd}			-	2.7	4.1	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 25 V, I_D = - 4.7 A, R_g = 24 Ω, R_D = 5.6 Ω, see fig. 10[b]		-	6.1	9.2	ns
Rise Time	t_r			-	47	71	
Turn-Off Delay Time	$t_{d(off)}$			-	13	20	
Fall Time	t_f			-	39	59	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.0	-	nH
Internal Source Inductance	L_S			-	6.0	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	- 1.1	A
Pulsed Diode Forward Current[a]	I_{SM}			-	-	- 8.8	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = - 0.7 A, V_{GS} = 0 V[b]		-	-	- 5.5	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = - 4.7 A, dI/dt = 100 A/μs[b]		33	75	160	ns
Body Diode Reverse Recovery Charge	Q_{rr}			0.090	0.22	0.52	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

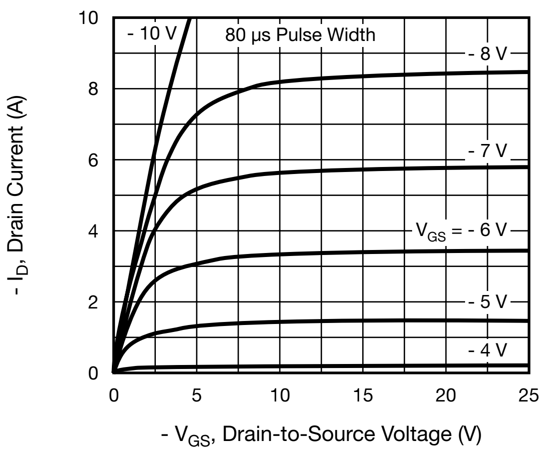


Fig. 1 - Typical Output Characteristics

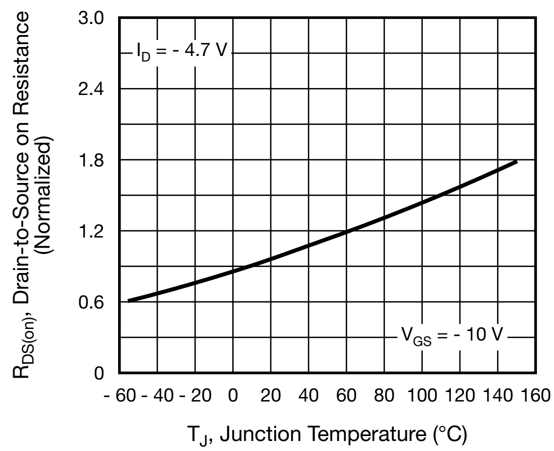


Fig. 4 - Normalized On-Resistance vs. Temperature

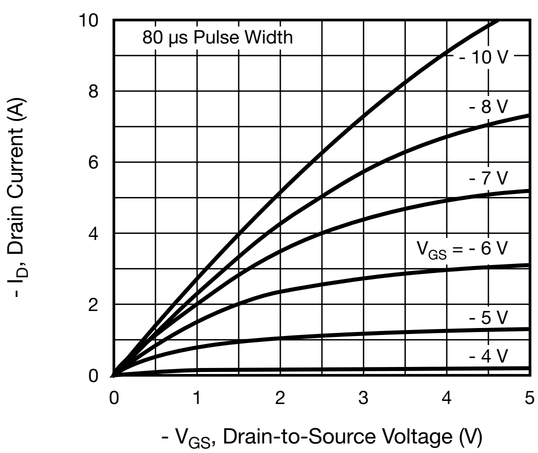


Fig. 2 - Typical Output Characteristics

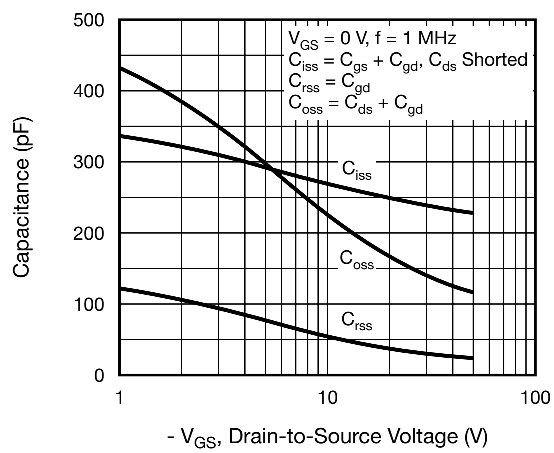


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

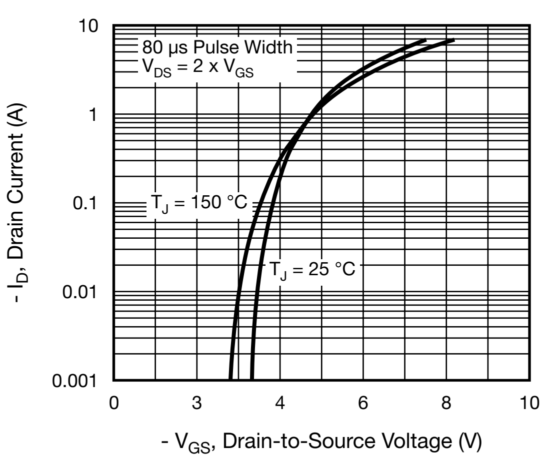


Fig. 3 - Typical Transfer Characteristics

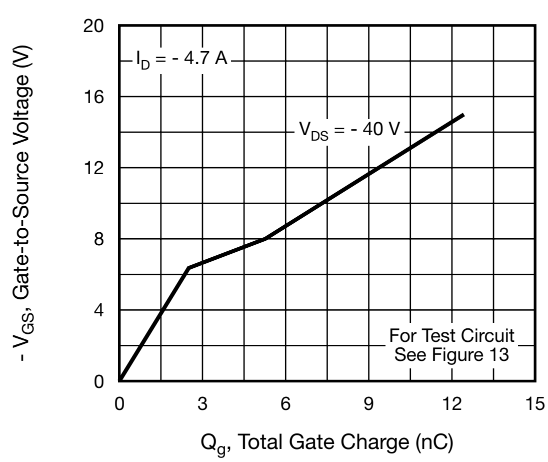


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

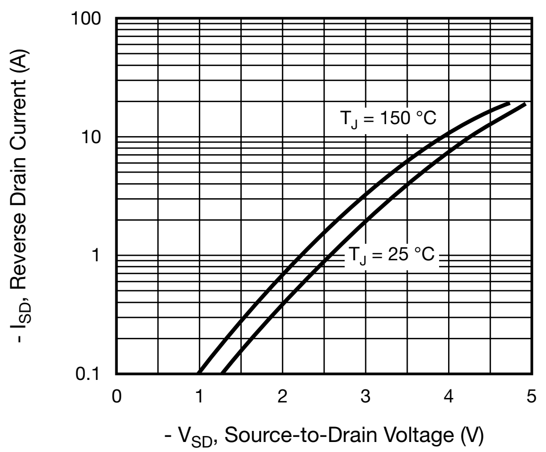


Fig. 7 - Typical Source-Drain Diode Forward Voltage

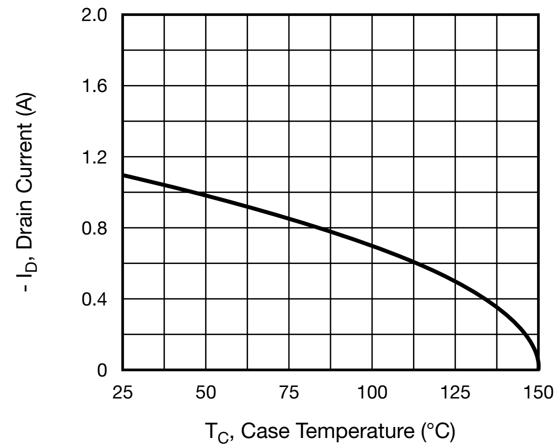


Fig. 9 - Maximum Drain Current vs. Case Temperature

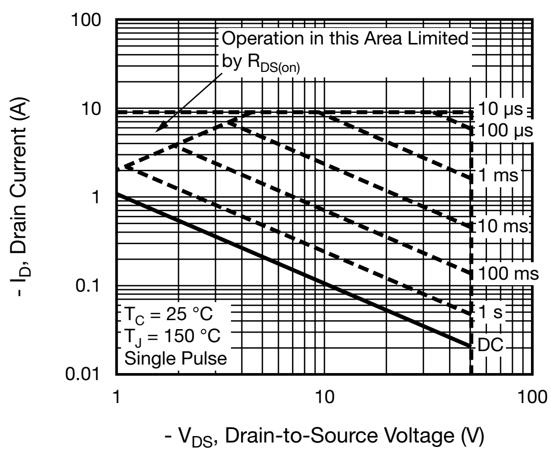


Fig. 8 - Maximum Safe Operating Area

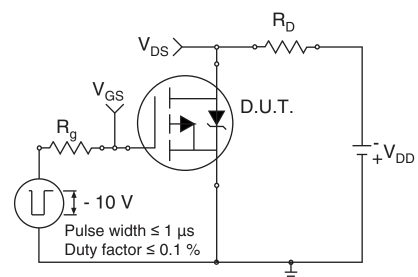


Fig. 10a - Switching Time Test Circuit

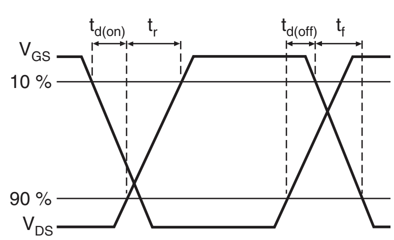


Fig. 10b - Switching Time Waveforms

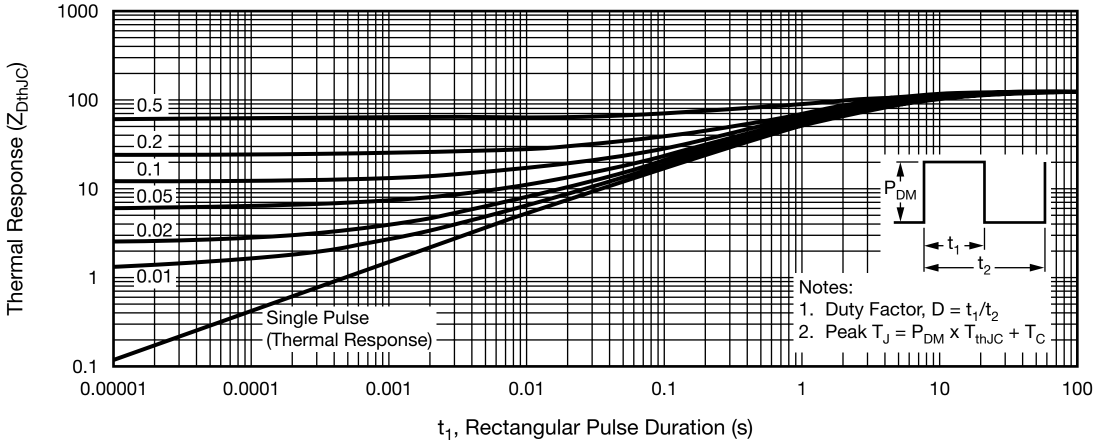


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

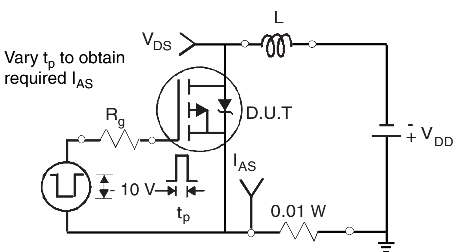


Fig. 12a - Unclamped Inductive Test Circuit

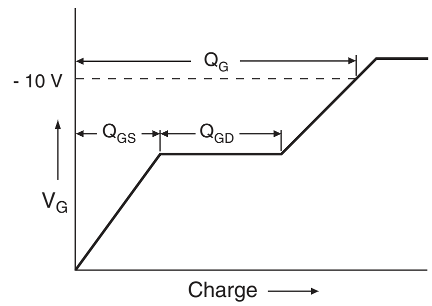


Fig. 13a - Basic Gate Charge Waveform

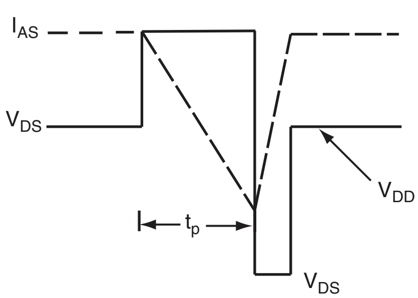


Fig. 12b - Unclamped Inductive Waveforms

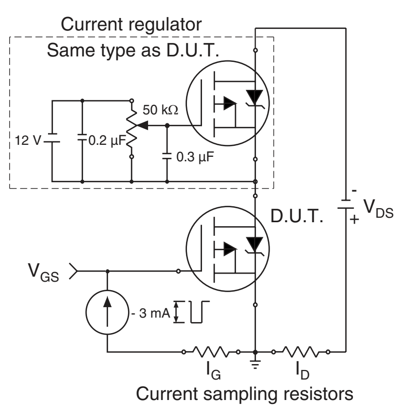
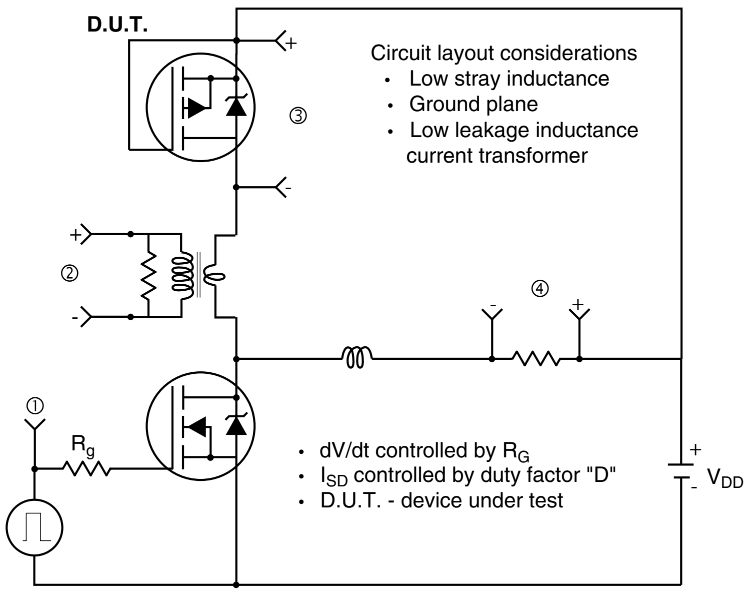
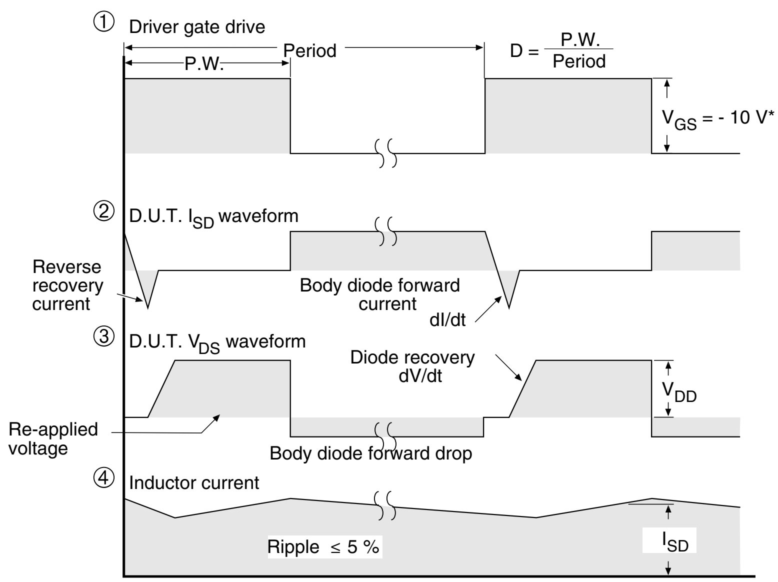


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



• Compliment N-Channel of D.U.T. for driver



* V_{GS} = - 5 V for logic level and - 3 V drive devices

Fig. 14 - For P-Channel

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